IN THE CLAIMS:

All pending claims are reproduced below. Please amend claims 17, 24, 27, 30 and 38 as set forth below.

1-16. Canceled.

17. (Currently Amended) A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a data block, comprising:

a plurality of cores, each having input data and output data, wherein the input data ~~for each core~~ includes external data and ~~output data~~ feedback data output from selected ones of the cores~~.~~, and wherein the plurality of cores includes

a first core having a first input, a second input and an output for performing forward DCT and IDCT operations, the first input of the first core coupled to receive external data, and

a second core having a first input, a second input and an output for performing forward DCT and IDCT operations, the first input of the second core coupled to receive external data, the second input of the second core coupled to the output of the first core and the output of the second core coupled to the second input of the first core to provide feedback data.

18. (Original) The DCT/IDCT circuit according to Claim 17, further comprising:

a sequence generator coupled to each core.

19. (Original) The DCT/IDCT circuit according to Claim 17, wherein the selected ones of the cores comprises four cores.

20. (Original) The DCT/IDCT circuit according to Claim 17, wherein the external data comprises the data block, the data block including prediction data processed by an MEC engine communicatively coupled to the DCT/IDCT circuit.

21. (Original) The DCT/IDCT circuit according to Claim 17, wherein the external data comprises the data block, the data block including reconstruction data processed by an inverse quantizer module communicatively coupled to the DCT/IDCT circuit.

22. (Original) The DCT/IDCT circuit according to Claim 17, wherein the plurality of cores comprises 8 cores.

23. (Original) The DCT/IDCT circuit according to Claim 17, wherein the plurality of cores comprises four types of cores.

24. (Currently Amended) The DCT/IDCT circuit according to Claim 23, wherein a first type of core includes a main register for storing the input data and the feedback data.

25. (Original) The DCT/IDCT circuit according to Claim 23, wherein a second type of core includes a first pair of lookup tables, and a third type of core includes a second pair of lookup tables.

26. (Original) The DCT/IDCT circuit according to Claim 23, wherein a fourth type of core includes two pairs of lookup tables.

27. (Currently Amended) A DCT circuit enabling forward discrete cosine transform of a data block, comprising:

a plurality of cores, each having input data and output data, wherein the input data ~~for each core~~ includes external data and ~~output data~~ feedback data output from selected ones of the cores~~.~~, and wherein the plurality of cores includes

a first core having a first input, a second input and an output for performing forward DCT operations, the first input of the first core coupled to receive external data, and

a second core having a first input, a second input and an output for performing forward DCT operations, the first input of the second core coupled to receive external data, the second input of the second core coupled to the output of the first core and the output of the second core coupled to the second input of the first core to provide feedback data.

28. (Original) The DCT circuit according to Claim 27, further comprising:

a sequence generator coupled to each core.

29. (Original) The DCT circuit according to Claim 27, wherein the selected ones of the cores comprises four cores.

30. (Currently Amended) An IDCT circuit enabling inverse discrete cosine transform of a data block, comprising:

a plurality of cores, each having input data and output data, wherein the input data ~~for each core~~ includes external data and ~~output data~~ feedback data output from selected ones of the cores~~.~~, and wherein the plurality of cores includes

a first core having a first input, a second input and an output for performing IDCT operations, the first input of the first core coupled to receive external data, and

a second core having a first input, a second input and an output for performing IDCT operations, the first input of the second core coupled to receive external data, the second input of the second core coupled to the output of the first core and the output of the second core coupled to the second input of the first core to provide feedback data.

31. (Original) The IDCT circuit according to Claim 30, further comprising:

a sequence generator coupled to each core.

32. (Original) The IDCT circuit according to Claim 30, wherein the selected ones of the cores comprises four cores.

33 - 37 Canceled.

38. (Currently Amended) A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a data block, comprising:

means for selecting one of input data of the data block received and a sum of said input data and feedback data, wherein the feedback data is generated external to the means for selecting, in order to provide first output data;

coupled to the means for selecting, means for determining first partial products based on the input data, the first output data and the feedback data;

coupled to the means for selecting and the means for determining first partial products, means for determining an intermediate result based on a sum of the first partial products; and

coupled to the means for selecting, the means for determining first partial products, and the means for determining an intermediate result, means for providing the intermediate result as an operand added to second partial products to obtain a final result.

39. (Original) The DCT/IDCT circuit according to Claim 38, further including means for obtaining the final result within two clock cycles.

40. (Original) A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a data block, comprising:

means for receiving input data associated with the data block;

coupled to the means for receiving, first means for selecting one of the input data and a sum of the input data and feedback data to provide first output data;

coupled to the first means, second means for determining a sum of first partial products based on the input data, the feedback data, and first coefficient data to provide second output data;

coupled to the means for receiving input data, third means for determining a sum of second partial products based on the input data, the feedback data, and second coefficient data to provide third output data;

coupled to the means for receiving input data, fourth means for determining a sum of additional partial products based on the input data, the feedback data, and additional coefficient data to provide third output data; and

means for outputting the first output data, the second output data and the third output data collectively representing a result of one of the forward discrete cosine transform and the inverse discrete cosine transform.